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# A New Structure of High Voltage Gain SEPIC Converter for Renewable Energy Applications

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**ABSTRACT** The paper proposes a new structure of SEPIC with high voltage gain for renewable energy applications. The proposed circuit is designed by amalgamating the conventional SEPIC with a boosting module. Therefore, the converter benefits from various advantages that the SEPIC converter has, such as continuous input current. Also, high voltage gain and input current continuity make the presented converter suitable for renewable energy sources. The modified SEPIC converter (MSC) provides higher voltage gain compared to the conventional SEPIC and recently addressed converters with a single-controlled switch. The analysis of voltage gain in continuous current mode (CCM) and discontinuous current mode (DCM) is analyzed by considering the non-idealities of the semiconductor devices and passive components. The selection of the semiconductor devices depending on the voltage–current rating is presented along with the designing of reactive components. The numerical simulation and experimental work are carried out, and the obtained results prove the feasibility of the MSC concept and the theoretical analysis.

**INDEX TERMS** DC-DC converter, energy conversion, high voltage gain, SEPIC, renewable energy.

## NOMENCLATURE

$S$	Active switch	$(I_{LX})_{max}, (I_{LY})_{max}$ and $(I_{LZ})_{max}$	Maximum peak current through inductor $L_X, L_Y$ and $L_Z$ .
$L_X, L_Y$ and $L_Z$	Inductors		
$C_1, C_2$ and $C_3$	Capacitors	$I_{C1}, I_{C2}$ and $I_{C3}$	Average current through capacitor $C_1, C_2$ and $C_3$ .
$D_1, D_2$ and $D_3$	Diodes		
$V_{in}$ and $V_0$	Input and output voltage	$I_{D1}, I_{D2}$ and $I_{D3}$	Average current of diode $D_1, D_2$ and $D_3$ .
$V_{C1}, V_{C2}$ and $V_{C3}$	Average voltage across capacitor $C_1, C_2$ and $C_3$ .	$I_{in}$ , and $I_0$	Average input and output current
$V_{LX}, V_{LY}$ and $V_{LZ}$	Voltage across inductor $L_X, L_Y$ and $L_Z$ .	$\tau$	Normalized inductor time constant
$k$	Duty ratio	$\tau_B$	Boundary normalized inductor time constant
$(I_{LX})_{min}, (I_{LY})_{min}$ and $(I_{LZ})_{min}$	Minimum peak current through inductor $L_X, L_Y$ and $L_Z$ .	$T_S$ and $f_S$	Switching time and switching frequency
		$P_{in}$ and $P_0$	Input and output power
		$R$	Resistive load

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$(L_X)_{cri}$ , $(L_Y)_{cri}$ , and $(L_Z)_{cri}$	Critical values of inductor $L_X$ , $L_Y$ and $L_Z$ .
$\Delta I_{LX}$ , $\Delta I_{LY}$ , and $\Delta I_{LZ}$	Peak to peak ripple currents of inductor $L_X$ , $L_Y$ and $L_Z$ .
$\Delta V_{C1}$ , $\Delta V_{C2}$ , and $\Delta V_{C3}$	Peak to peak ripple voltage of capacitor $C_1$ , $C_2$ and $C_3$ .
$r_{LX}$ , $r_{LY}$ , and $r_{LZ}$	Equivalent series resistance of inductor $L_X$ , $L_Y$ and $L_Z$ .
$r_{D1}$ , $r_{D2}$ , and $r_{D3}$	ON state resistance of diode $D_1$ , $D_2$ and $D_3$ .
$V_{F1}$ , $V_{F2}$ , and $V_{F3}$	Internal forward voltage drop of diode $D_1$ , $D_2$ and $D_3$ .
$r_S$	ON state resistance of switch $S$
$\phi$ , $\varphi$ , and $\gamma$	Voltage drop contributed by inductor $L_X$ , $L_Y$ and $L_Z$ .
$\vartheta$	Voltage drop across switch $S$
$\zeta$ , $\psi$ , and $\sigma$	Voltage drop across the diodes $D_1$ , $D_2$ and $D_3$ .
$\eta$	Efficiency
$P_{loss}^S$ , $P_{loss}^D$ , $P_{loss}^L$ and $P_{loss}^C$	Power loss across the switch $S$ , diodes, inductors and capacitors.
$P_{sw-loss}^S$ , $P_{c-loss}^S$	Switching and conduction power loss by the switch.
$R_{ds(ON)}$	ON state resistance of switch $S$
$V_{DS}$ and $I_S$	Drain to source voltage and current across/through switch $S$
$t_r$ and $t_f$	Rising and falling switching time of switch $S$

## I. INTRODUCTION

The utilization of existed fossil fuels is tremendously increased in the last decade, which leads to environmental contaminations and increases the cost of the system [1]. These problems attracts the researcher to work on Renewable Energy Resources (RES) such as Photovoltaic (PV), wind turbine, fuel cells, etc. Among these RES, PV is gaining more attraction and become noticeable as consequence of its

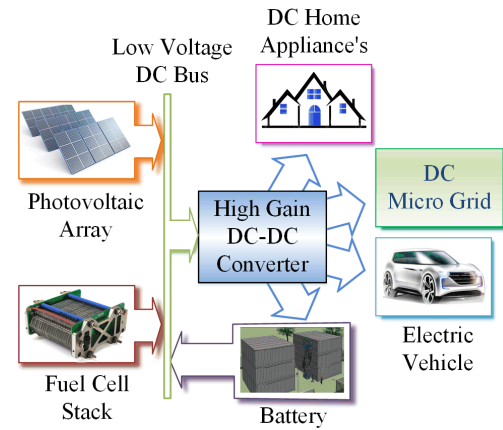


FIGURE 1. Modern smart grid architecture.

various advantages such as eco-friendly, abundant in nature, freely available, etc. However, the voltage generated from the PV modules is comparatively low and depends on the environmental conditions [2]. Therefore, in order to boost the PV voltage, series and parallel combinations of PV panels can be a solution to fulfill the load demand, which results in lower efficiency, high cost and large the size of the system [3], [4]. A high voltage gain DC-DC converter can be a practicable solution to boost the low voltage generated from PV. Fig. 1 shows the general architecture of modern smart DC grid system integrated with PV and fuel cell system. To meet the high voltage demand of DC home, electric vehicle, DC microgrid etc. high voltage gain converter is utilized as intermediate stage. The conventional boost, buck-boost, SEPIC, CUK, etc. can be utilized for high voltage applications at maximum duty ratio, but that decreases the efficiency and affects the functionality of converter [5], [6]. Recently, various high voltage gain DC-DC converters have been proposed with utilization of reactive components in boosting stages [7], [8]. In isolated DC-DC converter, High-Frequency Transformer (HFT) adopted to boost the input voltage by adjusting its turn ratio [9], [10]. Nevertheless, voltage based isolated DC-DC converters have high ripple in the input current and high voltage stress across the secondary side. Moreover, the leakage energy, bulky transformer and multistage power conversion process are the main shortcoming of the isolated converters [11]. Besides that, non-isolated DC-DC converters are the impeccable solution for PV application with high efficiency and compact size. In literature, various voltage-boosting techniques such as cascading of converters e.g. Quadratic Boost Converter (QBC) [12], voltage lift structure [13]–[19] or coupled inductor [20]–[22] have adopted with non-isolated converter to achieve high output voltage.

In the coupled inductor based converters, the output is controlled by adjusting turns ratio of inductor coil. The leakage inductance of the coupled inductor is inexorable which generates a spike in switch current and demands the clamping

circuit to suppress the current spike [23]. By utilizing the voltage lifting techniques/structures, numerous high gain DC-DC converters have been proposed in [9]–[19]. In [24], second order boost converter with voltage multiplier has been discussed. Presented converter has flexible structure and output voltage depends on the duty ratio as well as on the number of voltage multiplier level. Nonetheless, converter has low voltage gain even though with several numbers of voltage multiplier levels. Additionally, converter has very high input current ripple in the proportion of average input current that implies high-value inductor. In addition, converter has balancing issue of the voltage multiplying capacitors. Moreover, efficiency is decreasing with increasing number of level by the effect of the uncontrolled diodes. A switched capacitor based high gain DC-DC converter with multiple inductors and capacitors has been present in [24]. The presented converter shows the good regulation with lower voltage gain in comparison to the number of components. In [11], high gain switched capacitor DC-DC converter with the active network has been presented. The converter achieves high gain with pulsating current and poor regulation. The converter controlled with two switches and that make the complexity in the control scheme and affects the efficiency. Additionally, discontinues input current is another drawback of the circuitry which proves the minimum utilization of the sources [25].

## II. MODIFIED SEPIC CONVERTER

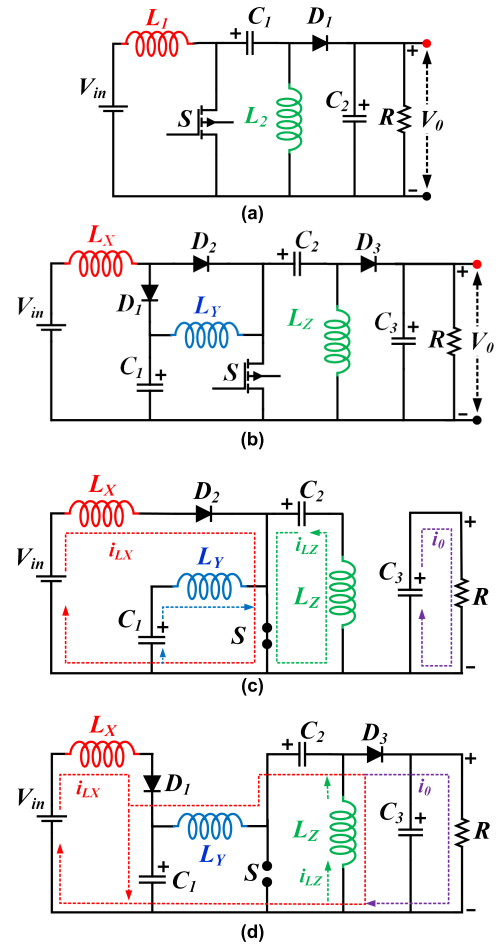
In this paper, a new structure of single switch non-isolated high gain SEPIC is introduced for high voltage application. The MSC has single input-output port and derived by transforming the classical SEPIC as shown in Fig. 2(a). Fig. 2(b) shows the power circuit of MSC consisting three inductors ( $L_X$ ,  $L_Y$  and  $L_Z$ ), three capacitors ( $C_1$ ,  $C_2$  and  $C_3$ ) and three diodes ( $D_1$ ,  $D_2$  and  $D_3$ ) which are controlled by single switch  $S$  with switching frequency ( $f_s$ ). In the MSC, inductor  $L_Y$  and capacitor  $C_1$  serve as a voltage-boosting element in addition with two diodes. The key features of the proposed MSC are; 1) operates with single switch that reduces the complexity of control circuitry, 2) continuous input current, 3) high voltage gain, 4) maximum utilization of input source.

### A. CCM OPERATION AND ANALYSIS

In order to explain the steady state operation, some assumptions are to be consider as: all components to be ideal and all capacitors should be large enough to achieve constant voltage. The MSC controlled by single switch  $S$ , hence the converter operates in two different modes as mode-I ( $t_0$  to  $t_1$ ) and mode-II ( $t_1$  to  $t_2$ ) as shown in Fig. 2(c) and (d) respectively. Where  $k$  is duty ratio and  $T_S = 1/f_s$  is the time required to complete one switching operation.

#### 1) MODE-I [ $t_0$ TO $t_1$ ]

In mode-I, three inductors are magnetized with current path as follow: inductor  $L_X$  from input supply ( $V_{in} - V_{LX} - D_2 - S - V_{in}$ ), inductor  $L_Y$  from capacitor  $C_1$  ( $V_{C1} - V_{LY} - S - V_{C1}$ ) and inductor  $L_Z$  from capacitor  $C_2$  ( $V_{C2} - S - V_{LZ} - V_{C2}$ ).



**FIGURE 2.** Power circuitry of (a) SEPIC and (b) MSC, CCM operating modes of MSC in (c) mode-I and (d) mode-II.

At the same instant, capacitor  $C_3$  reverse bias the diode  $D_3$  and transfer energy to the load as shown in Fig. 2(c). The characteristic waveforms of each component in mode-I are presented in Fig. 3.

$$\left. \begin{aligned} V_{LX} &= V_{in} \\ V_{LY} &= V_{C1} \\ V_{LZ} &= V_{C2} \end{aligned} \right\} \text{mode-I} \quad (1)$$

where,  $V_{LX}$ ,  $V_{LY}$ ,  $V_{LZ}$  are the voltages across inductor  $L_X$ ,  $L_Y$ ,  $L_Z$  respectively.  $V_{C1}$ ,  $V_{C1}$  are the voltage across capacitor  $C_1$ ,  $C_2$  respectively.

#### 2) MODE-II [ $t_1$ TO $t_2$ ]

In mode-II, all three inductors are demagnetized as follow: inductor  $L_X$  along with input voltage ( $V_{in}$ ) charges the capacitor  $C_1$  ( $V_{in} - V_{LX} - D_1 - C_1 - V_{in}$ ). The combination of inductor  $L_Y$  and capacitor  $C_1$  charges to capacitor  $C_2$  through the path  $V_{C1} - V_{LY} - V_{C2} - D_3 - V_0 - V_{C1}$ . Also at the same time, inductor  $L_Z$  discharges through the load with following the path ( $V_{LZ} - D_3 - V_0$ ) as shown in Fig. 2(d). The characteristic waveforms of each component in mode-II



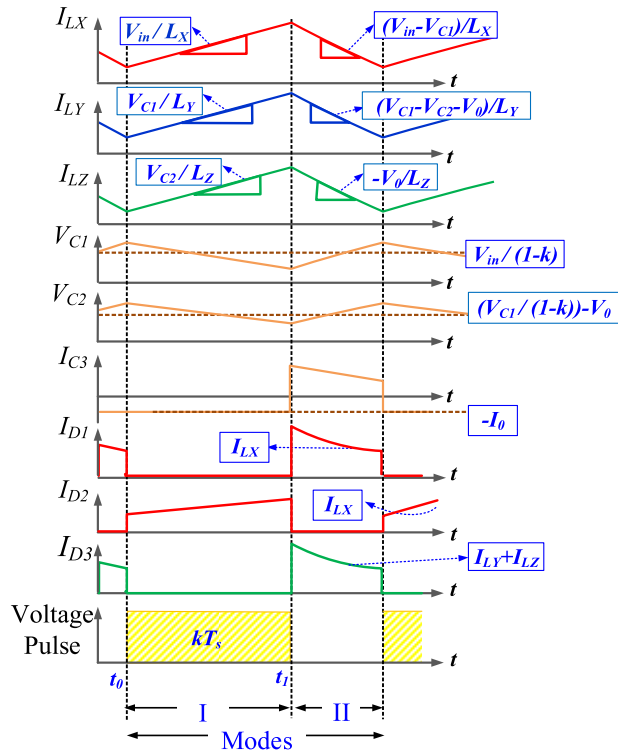


FIGURE 3. Characteristic waveforms of MSC in CCM.

are presented in Fig. 3

$$\left. \begin{aligned} V_{LX} &= V_{in} - V_{C1} \\ V_{LY} &= V_{in} - V_{L1} - V_{C2} - V_0 \\ V_{LZ} &= V_{C1} - V_{C2} - V_0 \end{aligned} \right\} \text{mode-II} \quad (2)$$

where,  $V_{C0}$  is the voltage across capacitor  $C_3$ . By applying Inductor Volt Second Balance (IVSB) principle for the inductors  $L_X$ ,  $L_Y$  and  $L_Z$ ,

$$\frac{V_{C1}}{V_{in}} = \frac{1}{1-k} \quad (3)$$

$$V_{C2} = \frac{V_{C1}}{1-k} - V_0 \quad (4)$$

$$\frac{V_0}{V_{C1}} = \frac{k}{1-k} \quad (5)$$

$$M_{CCM} = \frac{V_0}{V_{in}} = \frac{k}{(1-k)^2} \quad (6)$$

Equation (6) represents the voltage gain of the proposed converter in CCM mode.

## B. DCM OPERATION AND ANALYSIS

The MSC can be operates in Discontinuous Conduction Mode (DCM) as current through inductor/s reaches to zero levels individually or together as respective diode become reverse bias. The DCM operation of MSC is divided into three modes as mode-I, II and III. Where, mode-I and II have similar operating principle similar to CCM. Whereas, mode-III is a prolongation of Mode-II. Based on the inductor

current and respective diode operating state, the MSC can be work in three different possible DCM mode as mode-A, mode-B and mode-C. In mode-A, inductor  $L_X$  current  $(I_{LX})_{min}$  individually reach to zero level as diode  $D_1$  becomes reverse bias. In mode-B, diode  $D_1$  is forward bias and Diode  $D_3$  becomes reverse bias due to inductor  $L_Y$  and  $L_Z$  current  $((I_{LY})_{min}, (I_{LZ})_{min})$ . Similarly in mode-C, both diodes  $D_1$  and  $D_3$  become reverse bias by the effect of current through inductor  $L_X$ ,  $L_Y$  and  $L_Z$ . The power circuitry with respective current path in three possible DCM modes are shown in Fig. 4. Based on the three different possible modes, MSC has three different voltage gain in DCM. Hence, for simplicity the MSC is analyzed with mode-B DCM mode. The respective characteristic waveforms of each component are shown in Fig. 5.

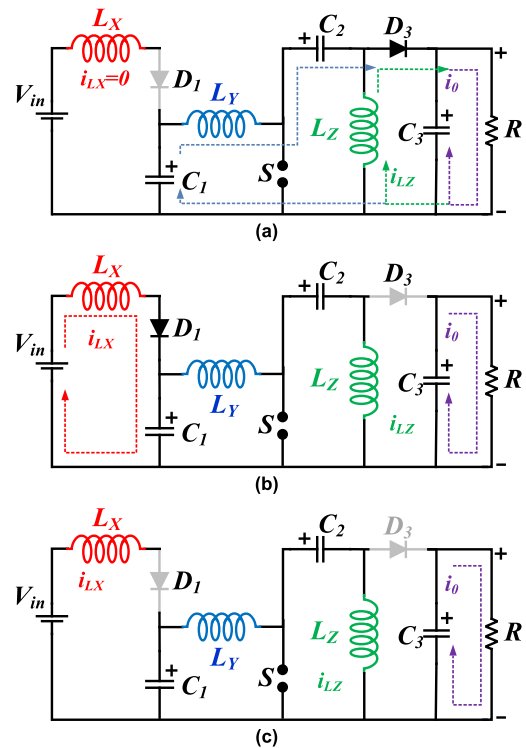


FIGURE 4. Possible DCM operating modes of MSC (a) mode-A, (b) mode-B, and (c) mode-C.

### 1) MODE-I [ $t_0$ TO $t_1$ ]

The equivalent circuit is same as mode I of CCM (Fig. 2(c)). In this mode, switches  $S$  turned ON. For this mode, the peak amplitude of current through inductor  $L_X$ ,  $L_Y$  and  $L_Z$  can be expressed as,

$$\left. \begin{aligned} (I_{LX})_{max} &= \frac{V_{in}kT_s}{L_X} \\ (I_{LY})_{max} &= \frac{V_{C1}kT_s}{L_Y} \\ (I_{LZ})_{max} &= \frac{L_Y}{V_{C2}kT_s} \end{aligned} \right\} \text{mode-I} \quad (7)$$

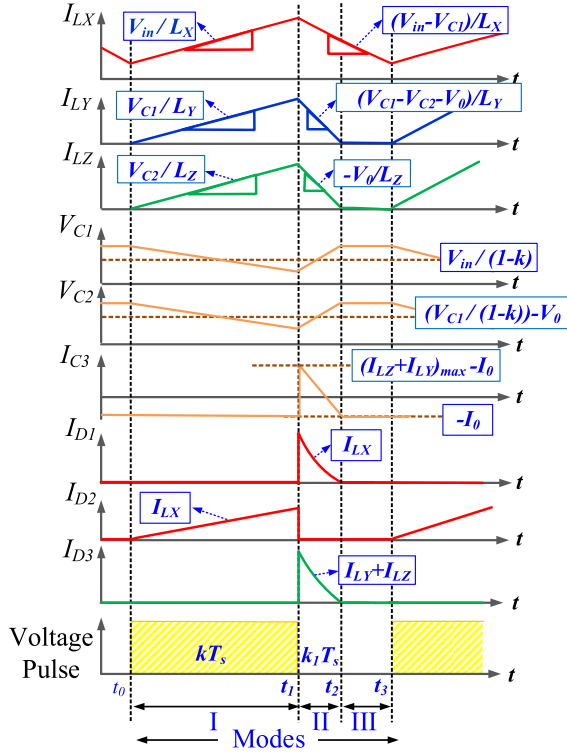


FIGURE 5. Characteristic waveforms of MSC in mode-B of DCM.

### 2) MODE-II [ $t_1$ TO $t_2$ ]

The equivalent circuit is same as mode II of CCM (Fig. 2(d)). In this mode, switches  $S$  turned OFF. For this mode, the peak amplitude of current through inductor  $L_X$ ,  $L_Y$  and  $L_Z$  can be expressed as,

$$\left. \begin{aligned} (I_{LX})_{\min} &= -\frac{(V_{in} - V_{C1}) k_1 T_s}{L_X} \\ (I_{LY})_{\min} &= -\frac{(V_{C1} - V_{C2} - V_0) k_1 T_s}{L_Y} \\ (I_{LZ})_{\min} &= \frac{V_0 k_1 T_s}{L_Z} \end{aligned} \right\} \text{mode-II} \quad (8)$$

### 3) MODE-III [ $t_2$ TO $t_3$ ]

The equivalent circuit of mode-III (mode-B) shown in Fig. 4(b). In this mode, switches  $S$  turned OFF. At the end of this mode, the energies stored in inductor  $L_Y$  and  $L_Z$  are zero. Hence, only energy stored in capacitor  $C_3$  is discharges to the load. Therefore, from (7) and (8),

$$k_1 = \frac{V_{C1} k}{V_0} \quad (9)$$

From Fig. 5, the average capacitor  $C_3$  current during each switching period is given by

$$\left. \begin{aligned} I_{C3} &= \frac{0.5 k_1 T_s (I_{LY} + I_{LZ})_{\max} - I_0 T_s}{T_s} \\ &= \frac{1}{2} k_1 (I_{LY} + I_{LZ})_{\max} - I_0 \end{aligned} \right\} \quad (10)$$

By substituting (7) and (9) in (10),  $I_{C3}$  is derived as

$$\frac{V_{C2} k^2 T_s}{2} \left( \frac{V_{C2} + V_{C1}}{L} \right) = \frac{V_0}{R} \quad (11)$$

From (3)-(6), (11) rearranged as

$$M_{DCM} = \frac{V_0}{V_{in}} = \sqrt{\frac{k^2}{(1-k)^2 \tau}}, \quad \tau = \frac{L}{RT_s} \quad (12)$$

where  $\tau$  is normalized inductor time constant.

Equation (12) represents the voltage gain of the proposed converter in DCM. Using (6) and (12), the boundary for CCM and DCM is derived as

$$\tau_B = (1-k)^2 \quad (13)$$

where  $\tau_B$  is boundary normalized inductor time constant.

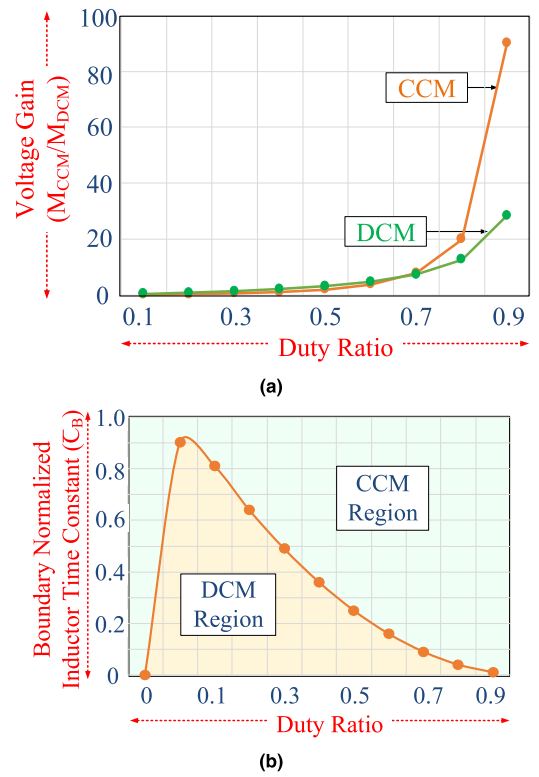


FIGURE 6. (a) Plot of voltage gain of MSC in CCM and DCM Vs. duty ratio and (b) plot of boundary normalized inductor time constant Vs. duty ratio.

The plot of voltage gain of MSC in CCM and DCM mode Vs. duty ratio is depicted in Fig. 6(a). Fig. 6(b) represents the graph of boundary normalized inductor time constant Vs. duty ratio. It is noteworthy that, if  $\tau$  is greater than  $\tau_B$ , then MSC operates in CCM. It is investigated that, after attaining the peak value there is decrement in normalized inductor time constant ( $\tau_B$ ) when duty ratio  $k$  is increased.

### C. DESIGN CONSIDERATION OF INDUCTORS

The selection of inductor is depends on the duty ratio, switching frequency and resistive load [3]. The current carrying

capacity and critical value of respective inductor to operate MSC in CCM is derived by;

$$(V_{LX})_{ON} = \left( L_X \frac{di_{LX}}{dt} \right)_{ON} = V_{in} \quad (14)$$

where  $I_{LX}$  is a current flowing through inductor  $L_X$  and  $dt$  is a change in time. Rearranging (14)

$$\left. \begin{aligned} L_X \frac{\Delta I_{LX}}{kT_S} &= V_{in} \\ \Delta I_{LX} &= \frac{kV_{in}}{f_S L_X} \end{aligned} \right\} \quad (15)$$

where  $f_S$  is a switching frequency to control the switch  $S$ . To find the input inductor  $L_X$  current, equate input power to output power.

$$P_{in} = P_0 = V_{in} I_{LX} = \frac{V_0^2}{R} \quad (16)$$

Rearranging the (16) and equating to (6)

$$I_{LX} = \frac{k^2 V_{in}}{(1-k)^4 R} \quad (17)$$

The maximum and minimum value of inductor current  $I_{LX}$  is derived as

$$(I_{LX})_{\max} = I_{LX} + \frac{\Delta I_{LX}}{2} = \frac{k^2 V_{in}}{(1-k)^4 R} + \frac{V_{in} k}{2L_X f_S} \quad (18)$$

$$(I_{LX})_{\min} = I_{LX} - \frac{\Delta I_{LX}}{2} = \frac{k^2 V_{in}}{(1-k)^4 R} - \frac{V_{in} k}{2L_X f_S} \quad (19)$$

To operate the converter in CCM mode, the inductor current must remain positive. To determine the boundary condition between CCM and DCM,  $(I_{LX})_{\min}$  is set to zero in (19)

$$(L_X)_{crit} = \frac{(1-k)^4 R}{2f_S k} \quad (20)$$

By (20) gives the critical value of inductor  $L_X$  below which ( $L_X < (L_X)_{crit}$ ) MSC work in DCM mode and work in CCM as  $L_X > (L_X)_{crit}$ .

With the same concept, the ripple content of  $I_{LY}$  can be derived from (4) as

$$\Delta I_{LY} = \frac{kV_{C1}}{f_S L_Y} = \frac{kV_{in}}{f_S (1-k) L_Y} \quad (21)$$

The MSC has cascaded connection of boost followed by SEPIC converter. As SEPIC receives the input from boost converter, the inductor  $L_Y$  current can be derived as,

$$\left. \begin{aligned} V_{C1} I_{LY} &= \frac{V_0^2}{R} \\ I_{LY} &= \frac{V_0^2}{V_{C1} R} = \frac{k^2 V_{in}}{(1-k)^3 R} \end{aligned} \right\} \quad (22)$$

The maximum and minimum peak value of inductor current  $I_{LY}$  can be derived as

$$(I_{LY})_{\max} = I_{LY} + \frac{\Delta I_{LY}}{2} = \frac{k^2 V_{in}}{(1-k)^3 R} + \frac{V_{in} k}{2(1-k) L_Y f_S} \quad (23)$$

$$(I_{LY})_{\min} = I_{LY} - \frac{\Delta I_{LY}}{2} = \frac{k^2 V_{in}}{(1-k)^3 R} - \frac{V_{in} k}{2(1-k) L_Y f_S} \quad (24)$$

To determine the boundary condition between CCM and DCM arises by the inductor  $L_Y$  current,  $(I_{LY})_{\min}$  is set to zero in (24)

$$(L_Y)_{crit} = \frac{(1-k)^2 R}{2f_S k} \quad (25)$$

With the same concept, the current ripple of inductor  $L_Z$  is derived from (1) and (9) as

$$\Delta I_{LZ} = \frac{kV_{C2}}{f_S L_Z} = \frac{kV_{in}}{f_S (1-k) L_Z} \quad (26)$$

In MSC, the current through inductor  $L_Z$  is load current and can be derived as

$$I_{LZ} = \frac{V_0}{R} = \frac{kV_{in}}{(1-k)^2 R} \quad (27)$$

The maximum and minimum value of inductor current ( $I_{LZ}$ ) are

$$(I_{LZ})_{\max} = I_{LZ} + \frac{\Delta I_{LZ}}{2} = \frac{kV_{in}}{(1-k)^2 R} + \frac{V_{in} k}{2(1-k) L_Z f_S} \quad (28)$$

$$(I_{LZ})_{\min} = I_{LZ} - \frac{\Delta I_{LZ}}{2} = \frac{kV_{in}}{(1-k)^2 R} - \frac{V_{in} k}{2(1-k) L_Z f_S} \quad (29)$$

By equating  $(I_{LZ})_{\min}$  to zero in (29), The critical value of inductor  $L_Z$  can be derived after rearranging as

$$(L_Z)_{crit} = \frac{(1-k) R}{2f_S} \quad (30)$$

#### D. DESIGN CONSIDERATION OF CAPACITORS

The value of capacitors depends on the voltage ripple ( $\Delta V_{C1}$  in  $C_1$ ,  $\Delta V_{C2}$  in  $C_2$  and  $\Delta V_{C3}$  in  $C_3$ ), duty ratio, load resistance, and switching frequency [3]. All three capacitors  $C_1$ ,  $C_2$  and  $C_3$  are selected with following expression as;

$$\left. \begin{aligned} | \Delta Q | &= \frac{V_{C1}}{R} k T_S = C_1 \Delta V_{C1} \\ \Delta V_{C1} &= \frac{V_{C1} k}{R C_1 f_S} \end{aligned} \right\} \quad (31)$$

The output stage consisting of the diode  $D_3$ , capacitor  $C_3$ , and the load resistor is the same as in the boost converter, so the output ripple voltage is same as the first stage boost converter and it is express as

$$\Delta V_{C3} = \frac{V_{C3} k}{R C_3 f_S} \quad (32)$$

The voltage variation in capacitor  $C_2$  is determined to from the circuit with the switch closed as presented in Fig. 3. From the definition of capacitance and accounting the magnitude of the charge,

$$\left. \begin{aligned} \Delta V_{C2} &= \frac{\Delta Q_{C2}}{C_2} = \frac{I_0 k T_S}{C_2} \\ &= \frac{V_0 k}{R f_S C_2} \end{aligned} \right\} \quad (33)$$

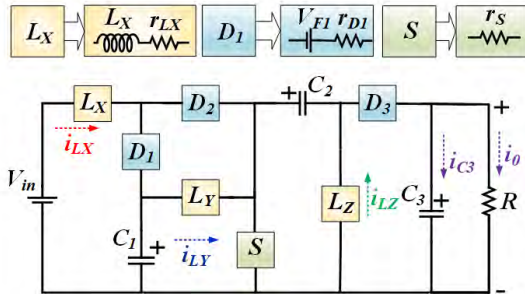


FIGURE 7. MSC with ESR of inductor, switch and voltage drop of diodes.

### III. EFFICIENCY ANALYSIS AND COMPARISON

#### A. EFFICIENCY ANALYSIS

In this sub-section, converter efficiency analysis is discussed. The equivalent circuit of MSC with non-idealities of circuit components i.e. internal resistance of respective components is shown in Fig. 7. Where  $r_{LX}$ ,  $r_{LY}$ ,  $r_{LZ}$  are the Equivalent Series Resistance (ESR) of inductor  $L_X$ ,  $L_Y$  and  $L_Z$  respectively. Similarly  $r_{D1}$ ,  $r_{D2}$ ,  $r_{D3}$  are internal resistance and  $V_{F1}$ ,  $V_{F2}$ ,  $V_{F3}$  are the forward voltage drop of three diodes  $D_1$ ,  $D_2$  and  $D_3$  respectively. Whereas,  $r_S$  is forward ON state resistance of a controlled switch  $S$ .

The equivalent voltage equations of three inductors with consideration of non-idealities in conducting and non-conducting state are

$$\left. \begin{aligned} V_{LX} &= V_{in} - i_{LX}(r_{LX} + r_S + r_{D2}) \\ &- i_{LY}r_S - i_{LZ}r_S - V_{F2} \\ V_{LY} &= V_{C1} - i_{LX}r_S - i_{LY}(r_{LY} + r_S) \\ &- i_{LZ}r_S \\ V_{LZ} &= V_{C2} - i_{LX}r_S - i_{LY}r_S \\ &- i_{LZ}(r_S + r_{LZ}) \end{aligned} \right\} \text{ON state} \quad (34)$$

$$\left. \begin{aligned} V_{LX} &= V_{in} - i_{LX}(r_{LX} + r_{D1}) \\ &- V_{F1} - V_{C1} \\ V_{LY} &= V_{C1} - i_{LY}(r_{LY} + r_{D3}) \\ &- i_{LZ}r_{D3} - V_{F3} - V_{C2} - V_0 \\ V_{LZ} &= -V_0 - i_{LZ}(r_{LZ} + r_{D3}) \\ &- i_{LY}r_{D3} - V_{F3} \end{aligned} \right\} \text{OFF state} \quad (35)$$

By the principle of IVSB, the resultant output voltage of MSC in terms of voltage drops across each component can be expressed as;

$$V_0 = \frac{kV_{in}}{(1-k)^2} - \left[ r_{LX}\phi + r_{LY}\varphi + r_{D2}\gamma + r_S\vartheta + r_{D1}\zeta + r_{D3}\sigma \right] \quad (36)$$

where,

$$\begin{aligned} \phi &= \frac{V_{in}k^3}{R(1-k)^5} \left\{ \text{voltage drop across inductor } L_X, \right. \\ \varphi &= \frac{V_{in}k^3}{R(1-k)^4} \left\{ \text{voltage drop across inductor } L_Y, \right. \\ \gamma &= \frac{kV_{in}}{R} \left\{ \text{voltage drop across inductor } L_Z, \right. \\ \vartheta &= \frac{kV_{in}}{R(1-k)^2} \left\{ \frac{(2-k)k^2}{(1-k)^2} + k^3(2-k) + 1 + (1-k)^2 \right\} \text{ by} \\ \text{switch } S, \\ \zeta &= \frac{kV_{in}}{R(1-k)^2} (k^2 + V_{F1}) \left\{ \text{voltage drop across diode } D_1, \right. \end{aligned}$$

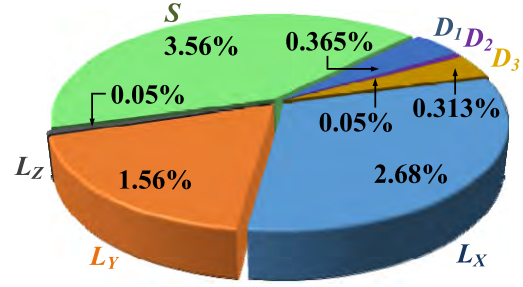


FIGURE 8. Voltage drop across each component with respect to output voltage in (%) at 0.7 duty ratio.

$$\psi = \frac{k^3 V_{in}}{R(1-k)^4} (k + V_{D2}) \left\{ \text{voltage drop across diode } D_2, \right.$$

$$\sigma = \frac{kV_{in}}{R(1-k)^2} (1 - k + V_{F3}) \left\{ \text{voltage drop across diode } D_3. \right.$$

The percentage of voltage drop across each inductor, diode and switch by their ESR with respect to output voltage is depicted in Fig. 8. It is observed that, switch  $S$  has higher contribution (3.56%) in voltage drop as compared to other circuit components at 0.7 duty ratio. However, diode  $D_2$  and inductor  $L_Z$  have relatively less contribution (0.05%) in voltage drop. The voltage gain and efficiency of the converter are affected by conduction loss due to the parasitic resistance of circuit element and switching loss by the semiconductor devices. Equation (37) gives the relation of output power with the efficiency. To evaluate the power losses and efficiency of MS converter, the losses can be calculated as for each component,

$$\eta = \frac{P_0}{P_0 + P_{loss}} = \frac{P_0}{P_0 + P_{loss}^S + P_{loss}^D + P_{loss}^L + P_{loss}^C} \quad (37)$$

where,  $P_{loss}^S$  is loss across switches,  $P_{loss}^D$  is loss across diodes,  $P_{loss}^L$  is loss by inductors, and  $P_{loss}^C$  is loss by capacitors. However, the switching and conduction loss of switches can be calculated based on the following equations for each switch.

$$\left. \begin{aligned} P_{loss}^S &= P_{c-loss}^S + P_{sw-loss}^S \\ P_{c-loss}^S &= R_{ds(on)} I_S^2 \\ P_{sw-loss}^S &= \frac{1}{2} V_{DS} I_S (t_r + t_f) f_s \end{aligned} \right\} \quad (38)$$

where,  $P_{c-loss}^S$  is a conduction loss contributed by switch,  $P_{sw-loss}^S$  is a switching loss contributed by switch,  $R_{ds(on)}$  is ON-state resistance,  $V_{DS}$  is a voltage across switch in OFF state,  $t_r$  and  $t_f$  are rising and falling time of switch and  $f_s$  represents the switching frequency of switch. With the help of (17), (22), (27), and (38) the expression of switching and conduction loss of MS converter is derived

$$\left. \begin{aligned} P_{sw-loss}^S &= \frac{k^2 V_{in}^2}{2R(1-k)^4} (t_r + t_f) f_s \\ P_{c-loss}^S &= R_{ds(ON)} \left[ \frac{kV_{in}}{R(1-k)^4} \right]^2 \end{aligned} \right\} \quad (39)$$

**TABLE 1.** Comparison of MSC with existing high gain converters.

Topologies	Number				$V_{DS}$	$M_{CCM}$
	$L$	$C$	$S$	$D$		
[5]	2	3	1	2	$V_0 / (1+k)$	$(1+k) / (1-k)$
[6]	4	6	1	3	$V_0 / 2$	$3k / (1-k)$
[11]	2	3	2	3	$V_0 / (2+k)$	$(2+k) / (1-k)$
[16]	1	3	1	3	$V_0 / 2$	$2 / (1-k)$
[20]	1	4	1	4	$V_0 / (3-k)$	$(3-k) / (1-k)$
[24]	2	3	2	3	$V_0 (1-k), kV_0$	$1 / k(1-k)$
[25]	2	3	1	2	$V_0 / 2k$	$2k / (1-k)$
[26]	3	3	1	5	$V_0 / k^2$	$k^2 / (1-k)^2$
QBC	2	2	1	3	$V_0$	$1 / (1-k)^2$
MSC	3	3	1	3	$V_0$	$k / (1-k)^2$

$L$ : inductor,  $C$ : capacitor,  $D$ : diode,  $S$ : switch,  
 $V_{DS}$ : voltage across switch,  $M_{CCM}$ : voltage gain ( $V_0/V_{in}$ )

**TABLE 2.** Simulation and hardware parameters of MS convert.

Parameter	Hardware Prototype
Input Supply	24 V
Switching frequency	50 kHz
Duty ratio	70 %
Power	100 W
Load (Resistive)	350 $\Omega$
Inductors ( $L_X$ , $L_Y$ and $L_Z$ )	$\approx 1$ mH, 15 A (shell type)
Cap. ( $C_1$ , $C_2$ and $C_3$ )	220 $\mu$ F, 350 V (electrolyte)
Switch	Power MOSFET (FDP19N40), $V_{DS}$ : 400V, $I_D$ : 9 A
Diodes	Power diode (STTH30R04)

The power loss by each diode can be calculated as

$$P_{loss}^D = (V_F \times I_{D(avg)}) + (r_D \times i_{D(rms)}^2) \quad (40)$$

$$= \frac{V_{in}k(1-k+k^2)}{R(1-k)^4}$$

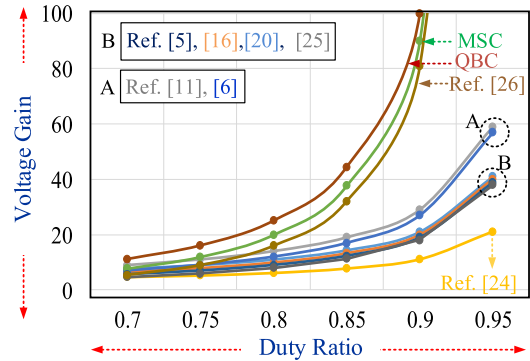
The power loss by the capacitors and inductors can be derived as

$$\left. \begin{aligned} P_{loss}^C &= r_C i_{C,rms}^2 \\ P_{loss}^L &= r_L i_{L,rms}^2 \end{aligned} \right\} \quad (41)$$

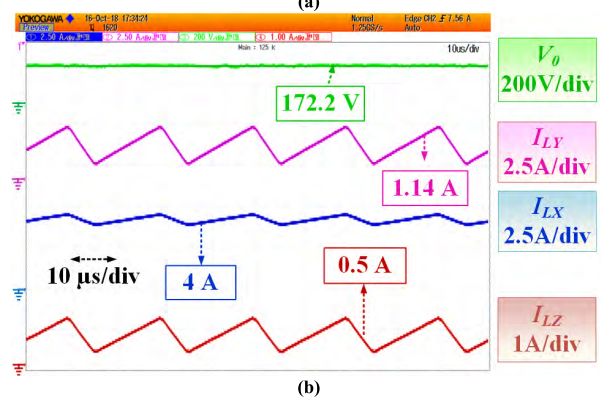
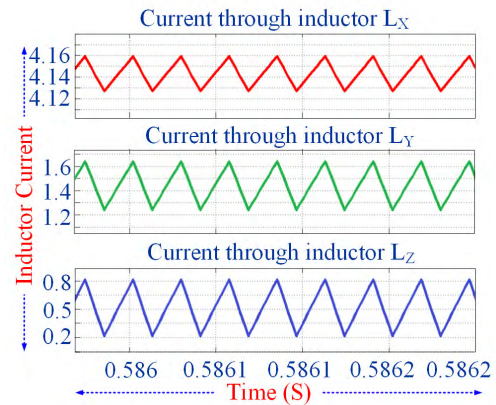
where  $r_C$  is ESR of capacitor. In this paper, magnetic loss by inductor and body diode conduction loss in switches are not considered.

## B. COMPARISON WITH RECENTLY ADDRESSED CONVERTERS

The proposed MSC is compared with recently addressed high gain converters as discussed in the literature. The comparison is made in term of number of active and passive components requirements, voltage stress across controlled switch ( $V_{DS}$ ), voltage gain ( $M_{CCM}$ ) as tabulated in Table 1. It is observed that, the MSC required less components as compared to other converters. From Fig. 9, it is noticed, the proposed converter gives higher voltage gain as compared to other converters.



**FIGURE 9.** Graph of voltage gain of recently addressed converter and MSC Vs duty ratio.

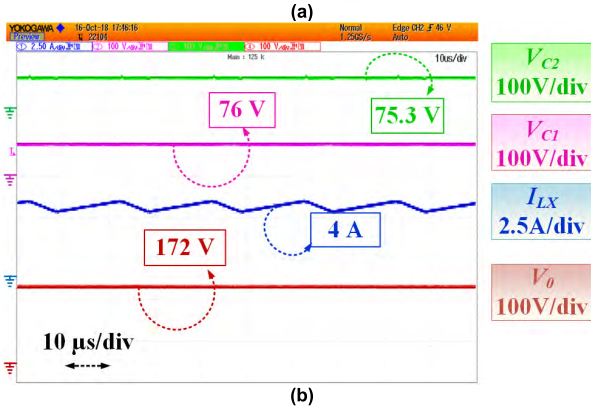
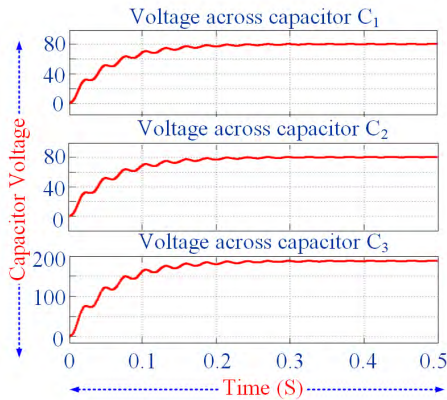


**FIGURE 10.** Waveform of current through inductor  $L_X$ ,  $L_Y$  and  $L_Z$  in (a) simulation and (b) hardware.

## IV. DISCUSSION ON SIMULATION AND HARDWARE RESULTS

The simulation and experimental work of proposed converter is performed to test its functionality. The MSC is implemented according to the aforementioned design procedure with the parameters given in Table 2. To operate the converter in CCM, the inductors  $L_X$ ,  $L_Y$  and  $L_Z$  values are selected more than respective critical value as derived in (14), (15) and (16), respectively. The gate pulse with 70 % duty ratio is generated through Virtex-5 FPGA. Fig. 10(a) depicts the simulation result waveform of inductor  $L_X$ ,  $L_Y$  and  $L_Z$  current.

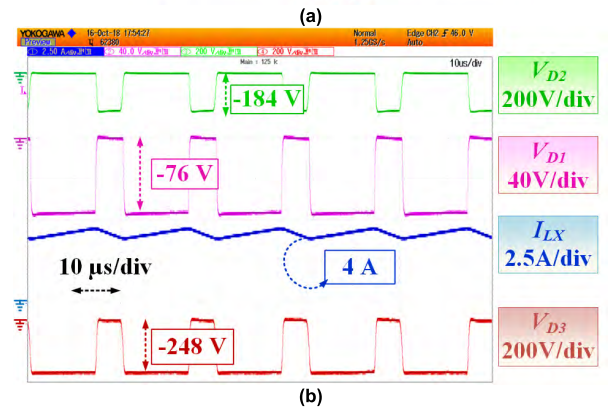
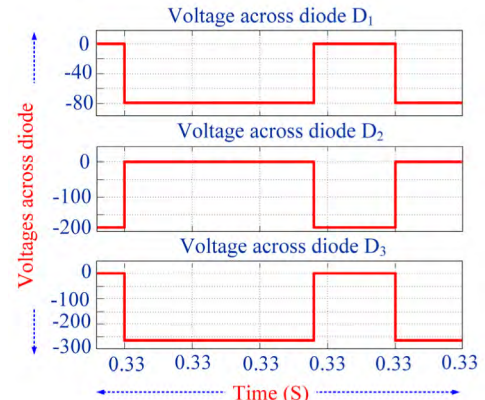




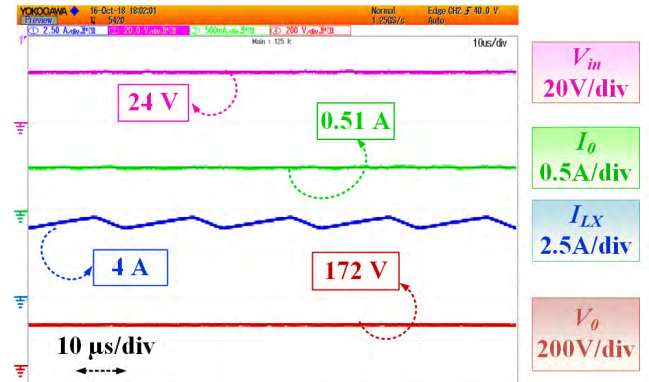
**FIGURE 11.** Waveform of voltage across capacitor  $C_1$ ,  $C_2$  and  $C_3$  in (a) simulation and (b) hardware.

It is observed that, inductor  $L_X$ ,  $L_Y$  and  $L_Z$  carry 4 A, 1.4 and 0.5 A (average) current. Whereas, Fig. 10(b) shows the experimental result waveform of output voltage ( $V_0$ ), inductor  $L_Y$  current ( $I_{LY}$ ),  $L_X$  ( $I_{LX}$ ) and  $L_Z$  ( $I_{LZ}$ ) current from top to bottom. During mode-I, current through all three inductors are increasing with positive slope at the same instant. Whereas, in mode-II, it starts decreasing with negative slope as expected. Fig. 11(a) depicts the simulation results waveform of capacitor  $C_1$ ,  $C_2$  and  $C_3$  voltage. It is observed that, +80 V is developed across the both capacitor  $C_1$  and  $C_2$ . Also, non-inverted 186 V across the capacitor  $C_3$ .

Fig. 11(b) depicts the experimental waveform of voltage across the capacitor is  $C_2$  and  $C_1$ ; current through inductor  $L_X$  and voltage across capacitor  $C_3$  from top to bottom. A non-inverting 76 V, 75.3 V and 172 V is developed across capacitor  $C_1$ ,  $C_2$  and  $C_3$  respectively in steady state as observed from Fig. 11(b). Fig. 12(a) and (b) shows the blocking voltage across diode  $D_1$ ,  $D_2$  and  $D_3$  in reverse bias condition. In mode-I, It is observed that Peak Inverse Voltage (PIV) across diode  $D_1$  is equal to voltage across capacitor  $C_1$  and equal to 76 V. Whereas, PIV across diode  $D_3$  is equal to addition of voltage across capacitor  $C_2$  and  $C_3$  i.e. ( $V_{C2} + V_0 = 184V$ ). In mode-II, diode  $D_2$  is reverse bias and handle PIV equal to output voltage ( $V_0$ ) and equals to 172V. Fig. 13 depicts the hardware result waveform of input voltage ( $V_{in}$ ), output current ( $I_0$ ), inductor  $L_X$  current ( $I_{LX}$ ) and output voltage ( $V_0$ ) from top to bottom. It is noticed from experimental results,



**FIGURE 12.** Waveform of voltage across diode  $D_1$ ,  $D_2$  and  $D_3$  in (a) Simulation and (b) hardware.

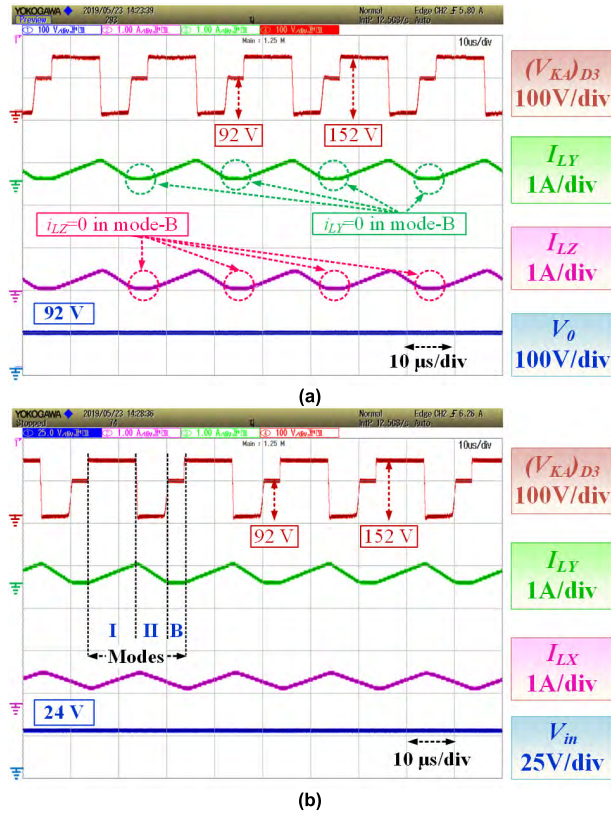


**FIGURE 13.** Experimental result of input voltage and current; output voltage and current.

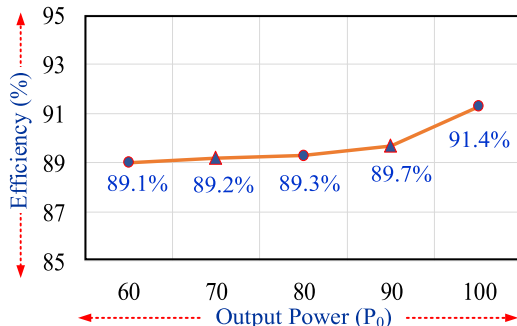
MSC operates with 24 V input supply and draw the input current ( $I_{LX} = I_{in}$ ) of 4 A with input power of 96 W. Furthermore, MSC develop 172 V at the load end ( $V_0$ ) with 0.51 load current ( $I_0$ ).

The DCM operation of proposed converter depends on the inductors value, duty ratio, value of resistive load and switching frequency. Therefore, the DCM mode can be achieved either by decreasing the duty ratio or switching frequency or by increasing the load resistance value. In this paper, the proposed converter operated in DCM operation by decreasing the duty ratio up to 60 % from 70 % without disturbing the other parameters. The experimental



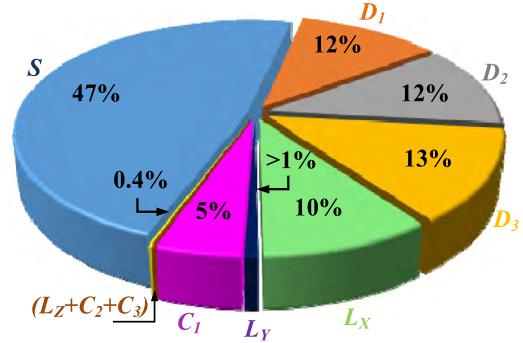


**FIGURE 14.** Experimental results of proposed converter in DCM mode (a) voltage across diode  $D_3$ , inductor  $L_Y$  and  $L_Z$  current and output voltage and (b) voltage across diode  $D_3$ , inductor  $L_Y$  and  $L_X$  current and input voltage.



**FIGURE 15.** Experimental efficiency curve at different power with constant load.

results of proposed converter in DCM mode are shown in Fig. 14. It is observed that, with decrease in duty ratio inductors  $L_X$ ,  $L_Y$  and  $L_Z$  current reaches to their maximum level in mode-I. In mode-II, inductors current ( $I_{LX}$ ,  $I_{LY}$  and  $I_{LZ}$ ) start decreasing. Whereas,  $I_{LY}$  and  $I_{LZ}$  reaches to zero level at the end of mode-II by the effect of reverse bias condition of diode  $D_3$ . It worth to note that from experimental results as shown in Fig. 14 (a) and (b), the proposed converter work in DCM mode (mode-B) due to the  $I_{LZ} = I_{LY} = 0$ . It is observed that, 92 V is developed at the load end at with 24 V input voltage at inductor time  $\tau = 0.142$ . Whereas, across diode  $D_3$  a 152 V (cathode to anode) voltage is appear as PIV.



**FIGURE 16.** Graph of power loss distribution across each component with respect to output power loss in (%) at 0.7 duty ratio.

Efficiency of proposed converter is experimentally analyzed for different power from 60 W to 100 W. It is observed that proposed converter operates with 89.1 % efficiency at 60 W load and 91.4 % at 100 W as shown in Fig. 15. With the help of (37)-(41), the power loss distribution across each component in the proposed converter calculated with ESR as ( $r_S = r_L = 0.2\Omega$ ,  $r_C = 0.1\Omega$ ,  $r_D = 0.01\Omega$  and  $V_F = 0.9V$ ). The power loss distribution across the each components is calculated and graphically shown in Fig. 16 with respect to output power loss. It is observed that, the maximum power loss is contributed by switch (47%). Whereas, capacitor  $C_2$ ,  $C_3$  and inductor  $L_Z$  have very less contribution ( $>1\%$ ) in power loss as compared to other components.

## V. CONCLUSION

A new structure of high gain modified SEPIC DC-DC converter has been introduced for renewable energy applications. High voltage gain and continuous input current are the advantages of MSC. The working principle of MSC in CCM and DCM mode has been presented. Additionally, the mathematical voltage gain derivation in CCM and DCM mode with non-idealities consideration and parameter design has been shown sequentially. Also, overall comparison between MSC and other non-isolated single switch converters has been addressed. The performance of the proposed converter is tested with numerical simulation and hardware implementation for 100 W prototype model. The results are shown for 172 V output from 24 V input supply with a gain of almost 8. According to the obtained results, it can be concluded that the proposed converter is well suited for high voltage renewable energy applications.

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